

AMENDMENT  
Serial No. 10/644,211

YOR920030266US1  
April 15, 2005

**AMENDMENTS TO THE CLAIMS:**

The below listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (currently amended) An integrated circuit (IC) comprising:
  - a plurality of functional units selectively communicating with each other;
  - a plurality of logic circuits connected together in ones of said plurality of functional units, connected said logic circuits in each of said ones defining function therein;
  - selectable supply switching devices disposed at ones of said logic circuits selectively supplying power and alternately isolating connected said logic circuits, said selectable supply switching devices turning on at a threshold voltage having a magnitude greater than like devices in [[is]] said logic circuits, wherein said devices are field effect transistors (FETs), ones of said selectable supply switching devices are p-type FETs (PFETs) connected between a supply line (V<sub>dd</sub>) and an intermediate supply line;  
a decoupling capacitor at each said intermediate supply line; and
  - a switchable bias supply at each selectable supply switching device selectively reducing threshold voltage magnitude responsive to said each selectable supply switching device supplying power.
2. (canceled).
3. (currently amended) An IC as in claim 1 [[2]], wherein whenever ones of said selectable supply switching devices are supplying power to said connected logic circuits, said switchable bias supply at said ones provides a body bias of V<sub>dd</sub> - 0.7V to said one.

AMENDMENT  
Serial No. 10/644,211

YOR920030266US1  
April 15, 2005

4. (original) An IC as in claim 3, wherein whenever ones of said selectable supply switching devices are isolating said connected logic circuits, said switchable bias supply at said ones provides a body bias of  $V_{dd}$  to said one, whereby leakage current in and off said one is substantially reduced with said body bias of  $V_{dd}$  over said off ones with body bias at  $V_{dd} - 0.7V$ .

5. (currently amended) An IC as in claim 1 [[2], wherein at least one said intermediate supply line is connected to two or more of said logic circuits.

6. (canceled)

7. (currently amended) An integrated circuit (IC) comprising:

a plurality of functional units selectively communicating with each other;  
a plurality of logic circuits connected together in each of said plurality of functional units, connected said logic circuits in each functional unit defining function in said each unit; [[and]]

selectable supply switching devices disposed at ones of said logic circuits selectively alternately supplying power and isolating connected said logic circuits, said selectable supply switching devices being a high threshold device turning on at a threshold voltage having a magnitude greater than at least one like device in devices is said logic circuits, each said of selectable supply switching devices being one in a series of stacked high threshold devices, wherein said devices are field effect transistors (FETs), ons of said selectable supply switching devices are p-type FETs (PFETs) connected between a supply line ( $V_{dd}$ ) and an intermediate supply line; and  
a decoupling capacitor at each said intermediate supply line.

8. (canceled)

9. (currently amended) An IC as in claim 7 [[8]], wherein said selectable supply switching PFETs are each one of a pair series of stacked said high threshold PFETs, one

AMENDMENT  
Serial No. 10/644,211

YOR920030266US1  
April 15, 2005

of each of said pairs being connected to  $V_{dd}$  and the other of said pair being connected to said intermediate supply line.

10. (original) An IC as in claim 9, wherein at least one said intermediate supply line is connected to two or more of said logic circuits.

11. (canceled)

12. (currently amended) An IC as in claim 7 [[8]], wherein remaining ones of said selectable supply switching devices are n-type FETs (NFETs [[PFETs]]) connected between a supply return line (Gnd) and an intermediate return line.

14. (original) An IC as in claim 12, wherein said series stacked said high threshold devices comprises:

a plurality of high threshold PFET pairs, a first PFET of each of said PFET pairs being connected between  $V_{dd}$  and said intermediate supply line; and

a plurality of high threshold NFET pairs, a first NFET of each of said pairs being connected between Gnd and said intermediate return line.

15. (original) An IC as in claim 14, wherein ones of said first PFET are paired with a plurality of second PFETs.

16. (original) An IC as in claim 14, wherein ones of said first NFET are paired with a plurality of second NFETs.

17. (original) An IC as in claim 14, wherein a second PFET of said plurality of high threshold PFET pairs is a logic circuit PFET in one first supply switched logic circuit and a second NFET of said plurality of high threshold pairs is a logic circuit NFET in one second supply switched logic circuit.

AMENDMENT  
Serial No. 10/644,211

YOR920030266US1  
April 15, 2005

18. (original) An IC as in claim 17, wherein a logic path in at least one of said plurality of functional units comprises alternating first supply switched logic circuits and second supply switched logic circuits.

19 (canceled)

20. (currently amended) An IC as in claim 30 [[19]], wherein said selectable supply switching NFETs are each one of a pair series of stacked said high threshold NFETs, one of each of said pairs being connected to Gnd and the other of said pair being connected to said intermediate return line.

21. (original) An IC as in claim 20, wherein at least one said intermediate return line is connected to two or more of said logic circuits.

22. (canceled)

23. (original) An IC as in claim 7, wherein series of stacked said high threshold devices are tapered widest to narrowest with the widest said high threshold devices being disposed in said series nearest to a logic circuit output and the narrowest at supply connections.

24. (original) An IC as in claim 23, wherein tapered said series of stacked high threshold devices have a taper ratio of 4, each said high threshold devices in said tapered series being 4 times wider than its next adjacent narrower stacked said device.

25. (original) An IC as in claim 24, wherein said tapered series of stacked high threshold devices comprises 2 said high threshold devices.

26 – 29 (canceled)

AMENDMENT  
Serial No. 10/644,211

YOR920030266US1  
April 15, 2005

30. (new) An integrated circuit (IC) comprising:

a plurality of functional units selectively communicating with each other;  
a plurality of logic circuits connected together in each of said plurality of functional units, connected said logic circuits in each functional unit defining function in said each unit;  
selectable supply switching devices disposed at ones of said logic circuits selectively alternately supplying power and isolating connected said logic circuits, said selectable supply switching devices being a high threshold device turning on at a threshold voltage having a magnitude greater than at least one like device in said logic circuits, each said of selectable supply switching devices being one in a series of stacked high threshold devices, wherein said devices are field effect transistors (FETs), ones of said selectable supply switching devices are n-type FETs (NFETs) connected between a supply return line (Gnd) and an intermediate return line; and  
a decoupling capacitor at each said intermediate return line.